HD-PLC

Green Ubiquitous

# IEEE 1901 HD-PLC (High Definition Power Line Communication)


## Abstract

The growing penetration of the internet throughout the society has also brought advantages to SOHOs and home networks. As networks develop, the demand for more multimedia content has grown along with the demand for faster network equipment. It is also widely known that HD-PLC systems that do not require new cables to be installed are convenient for network use with portables, where reliability and speed are main factors in power line communication. The PLC adaptor and PLC module will enable ubiquitous home networking and include high-speed data transmission technology using home power lines. This report shows that the HD-PLC system ensures advantages through the link everywhere concept that features

1) No wiring needed (all power plugs perform as information plugs),
2) Easy connection (just plug-in and connect to network)
3) Achieving AV transmission (with high communication throughput and realizing QoS)


## 1. Introduction

At Panasonic Communications we provide users with the PLC adaptor and the PLC module which incorporates into their equipment so as to create ubiquitous home networks using high-speed data transmission technology via home power lines. In this paper we introduce the features of these devices, with a focus on the HD-PLC products, Physical Layer and Media Access Control Layer technology, which do not require additional wiring (all power outlets become data connections), allow easy connectivity (network connections are established merely by inserting the power plug), and provide AV transmission (fast communication throughput and QoS).

 

### 1.1. Overview of the IEEE 1901 HD-PLC IP

The HD-PLC IP system from Panasonic System Networks is composed of the MAC, PHY and associated blocks required to implement a complete HD-PLC solution. The MAC and the Modem are conformant to the Wavelet MAC/PHY of IEEE 1901 and co-existence specification (ISP)

The HD-PLC IP system consists of MAC software, MAC hardware and PHY hardware.

- The upper software portion of the HD-PLC MAC is implemented in ANSI 'C'.
- The lower software portion of the HD-PLC MAC is implemented in assembly and executes on microcode engines.
- The hardware portion of the HD-PLC MAC and the PHY are implemented as synthesizable cores in Hardware description language.

The IP system may be integrated into a single chip solution along with an application processor sub-system, or may be synthesized on a separate chip as a peripheral to the application processor sub-system.

Figure 1 shows a structural example of a separate chip. This chip is separated into a microcomputer processing section, a PHY processing section, and a MAC processing section. The LSI is connected to a PLC analog front-end, an Ethernet PHY, SDRAM (Synchronous Dynamic Random Access Memory) and Flash ROM (Flash Read Only Memory) as peripheral devices.

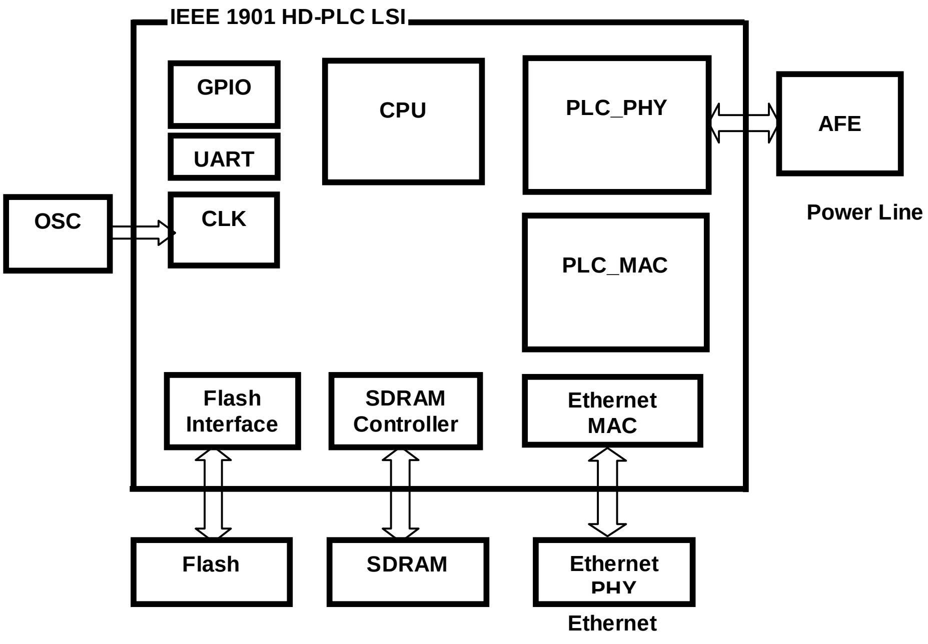


Fig. 1 LSI block Diagram

### 1.2. Examples of the HD-PLC LSI, Adaptor and Module

Table 1 lists the sample specifications of a PLC adaptor, and Figure 2 shows an external view of the PLC adaptor PLC-HP240EA, the PLC module board DRT-J520 and the PLC LSI KHN13200. The size of the module board is at roughly around 70 mm x 30 mm. The KHN13200 includes a fully integrated AFE with A/D, D/A converter and PGA (Programmable Gain Amp.).

Table 1 Specifications of the PLC Adaptor (PLC-HP240EA)

| | |
|---|---|
| Standard | IEEE 1901 HD-PLC |
| Frequency Band | 2 MHz ~ 28 MHz |
| Modulation | Wavelet OFDM (32 PAM to 2 PAM) |
| Transmission PHY Rate | 240 Mbps(theoretical maximum transmission rate) |
| Access Method | CSMA/CA, DVTP(Dynamic Virtual Token Passing) |
| Security | AES 128-bit Encryption by Auto Setting |
| Error Correction | Reed-Solomon and Convolutional/Viterbi or LDPC-CC |
| Power consumption | 2.3W |


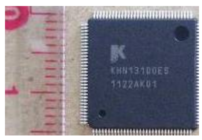

Fig. 2 Adaptor PLC-HP240EA (by I-O DATA) Module DRT-J520 (by MITSUMI ELECTRIC) LSI KHN13200 (by Kawasaki Microelectronics)

## 2. HD-PLC Physical Layer Technology

### 2.1. Overview of the Physical (PHY) Layer

The HD-PLC PHY uses Wavelet OFDM (Orthogonal Frequency Division Multiplexing) technology to provide highly efficient transmission and can coexist with existing systems (shortwave broadcasts and ham radio).

Highly efficient transmission is possible with Wavelet OFDM through appropriate modulation of the sub-carrier and having no GI (Guard Interval). Moreover, deep notches over -35 dBc (flexible notches) can be created at the desired bandwidth by not using arbitrary sub-carriers. In the HD-PLC, PHY speed of up to approximately 240 Mbps is achieved at a bandwidth of 26 MHz. In addition, high-quality, highly reliable communications are achieved even in poor quality home power transmission routes through the use of strong error correction coding and a diversity mode.

## 2.2. Time-Waveform in the Wavelet OFDM

In the FFT (Fast Fourier Transform) OFDM, a conventional technology, it was necessary to have a GI which was used to maintain orthogonality and a redundant signal for waveform rectification which was required to create a low side-lobe level in each sub-carrier. In Wavelet OFDM, the GI and the redundant signal for waveform rectification are absent; instead, a filter with a long impulse response is used. As a result, the time-waveform of each sub-carrier is transmitted in superposition while orthogonality is maintained, as shown in Figure 3. In the same fashion, orthogonality is maintained in each sub-carrier as well. In this fashion, the Wavelet OFDM represents a method appropriate for highly efficient transmission.

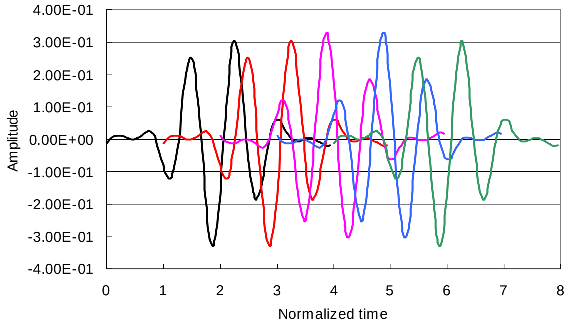


Fig. 3 Time-waveform of the sub-carrier

## 2.3. Wavelet OFDM Spectrum

Figure 4 shows the Wavelet OFDM spectrum. In the Wavelet OFDM, bandwidth is limited by a filter which has a long impulse response, as shown in Figure 3. As a result, a low side-lobe over -35 dBc can be readily achieved. Consequently, even if there is narrowband interference from existing systems, the effect is only present in some sub-carriers, and ICI (Inter-Carrier Interference) level can be suppressed.

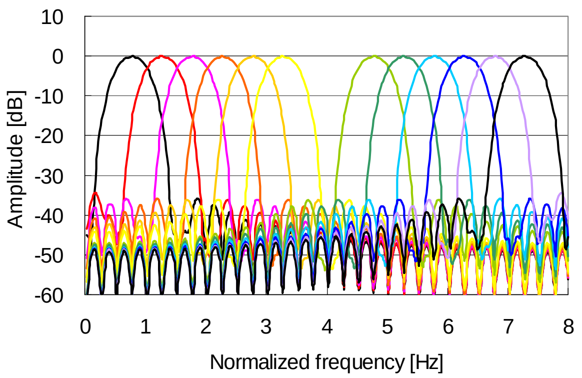


Fig. 4 Wavelet OFDM spectrum

A notch with attenuation over 35 dB can be easily created by not using sub-carriers present in an arbitrary frequency bandwidth, as shown in Figure 5 (in Figure 5, notches are formed in the North America amateur radio bandwidth).
In this manner, Wavelet OFDM, which can easily coexist with existing systems, is a good format for PLC.

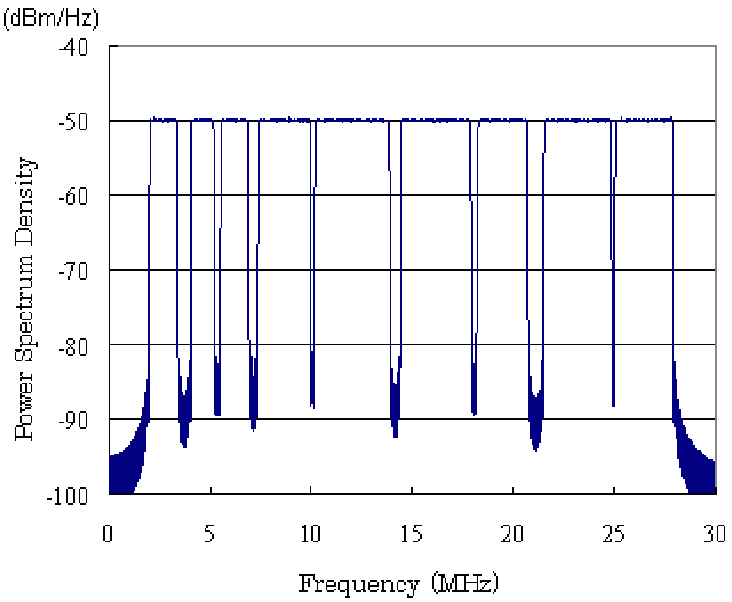


Fig. 5 HD-PLC spectrum

## 3. HD-PLC Media Access Control

### 3.1. Overview of Media Access Control (MAC)

HD-PLC MAC is an architecture that particularly emphasizes on AV transmission, and provides a function to maintain QoS (Quality of Service), a function to estimate transmission channels, and a function to improve transmission efficiency.

### 3.2. Quality of Service (QoS) Architecture

The HD-PLC QoS control function has a role in determining and controlling the schedule for channel access. Using Beacon frames, the controller notifies other stations of the medium access schedule up to the next Beacon frame. During each beacon interval there are three distinct blocks of time as shown in Fig 6. The first is the beacon extent, which is a fixed time period in which the HD-PLC Master terminal is required to send a Beacon frame. The second is the contention free period (CFP), which is used for transmission by HD-PLC terminals that require reserved bandwidth on a scheduled basis. The third is the contention period (CP), which provides a “best effort” service; this service might include preference settings for the transmitted frames. The HD-PLC MAC supports 16 levels of priority for each data frame transmitted. 8 of these priority levels are user specifiable. TDMA channel access is realized during a CFP period, but it is an optional service.

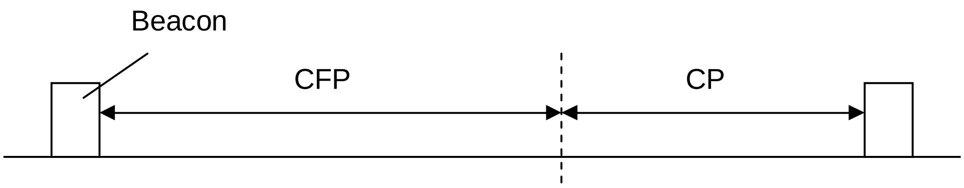


Fig. 6 Scheduling

### 3.3. CSMA/CA

The fundamental media access protocol of the HD-PLC is a procedure called carrier sense multiple access with collision avoidance (CSMA/CA). During the CP, three media access mechanisms work to reduce the collisions: 1) CSMA/CA access, 2) priority control CSMA/CA, and 3) Dynamic Virtual Token Passing (DVTP) access. For the easy realization of the Quality of Service (QoS), priority control CSMA/CA mechanism is provided on the basis of the CSMA architecture. The priority control CSMA/CA has an additional two state following CIFS (Contention Inter-Frame Space) in the contention period, the gap state and the CONTENTION state (as shown in Figure 7) and completely separate the transmission opportunity between Higher User Priority and other priorities. By using the GAP state, the higher User Priority data can contend without other lower User Priority data because the other lower User Priority data just wait until the end of the GAP state and does not participate in the contention with the Back off mechanism.

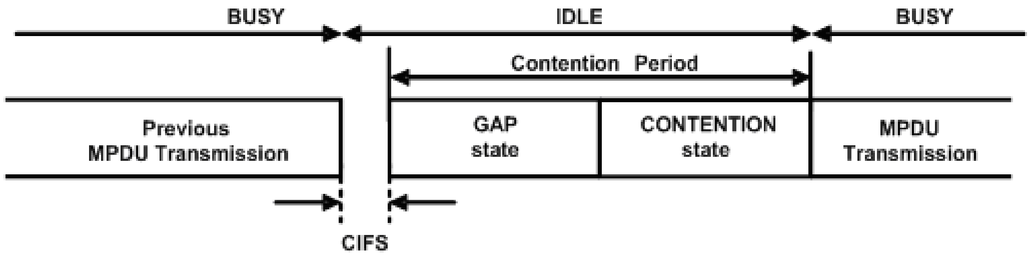


Fig. 7 Media State of priority control CSMA/CA

### 3.4. Dynamic Virtual Token Passing (DVTP)

DVTP (Dynamic Virtual Token Passing) is a distinctive media access mechanism based on the carrier sense and virtual token technique in which frame transmission arbitration is autonomously carried out by using slots, where the period after a data frame is divided into fixed-length time units (equivalent to the carrier detection time: 54 µs), and through this system collision avoidance on the network can be accomplished. When DVTP mechanism is available in a CP, IFS based priority control CSMA/CA is not available during the CP.

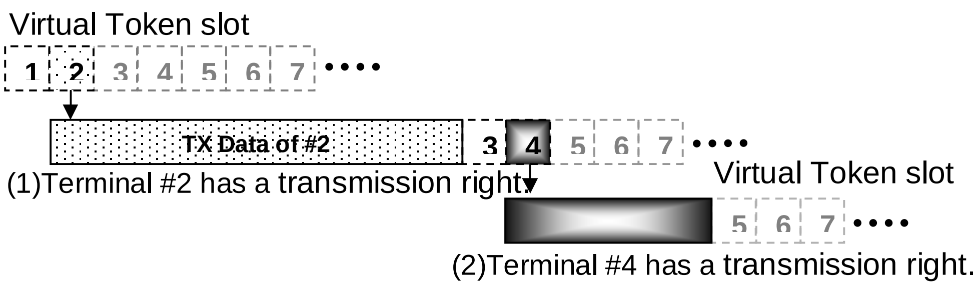


Fig. 8 Media access control by DTVP

 

### 3.5. Frame concatenation

As speed in the physical layer (PHY) increases, the time available for the payload in the frame decreases, and the gap, which requires a certain amount of time, between the header and frame becomes a huge overhead and hence it cannot be ignored. Thus, in HD-PLC MAC, overhead is reduced and transmission efficiency is improved by creating a frame with several Ethernet packets which allows creating one container block. A container block can consist of a maximum of 60 segment blocks, as shown in Figure 9. Each segment block can consist of up to 31 aggregated MSDU (MAC Service Data Unit).

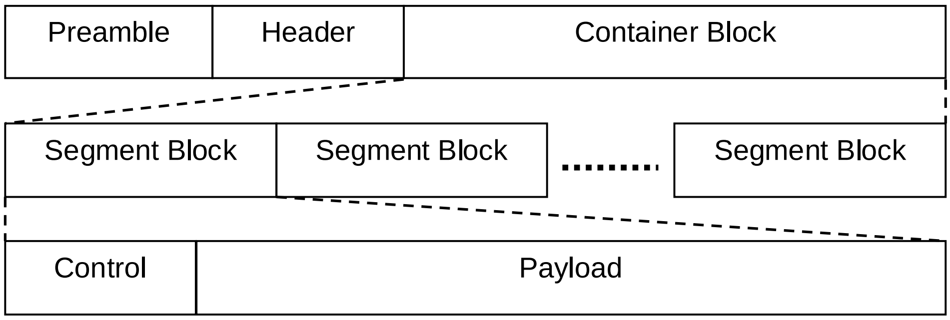


Fig. 9 Frame structure

Moreover, when an error occur, the efficiency is improved though selective repeat process. Figure 10 shows frames with eight segments. In the first frame, when an error occurs in segment blocks 2, 4, and 5, that information is sent from the reception side to the transmission side in the response frame. The response frame includes an NAK/ACK (Negative Acknowledgement / Acknowledgement) in all segment blocks. In the next frame, the data for 2, 4, and 5, where the errors occurred, are repeated, and the data from 9 onward is sent.

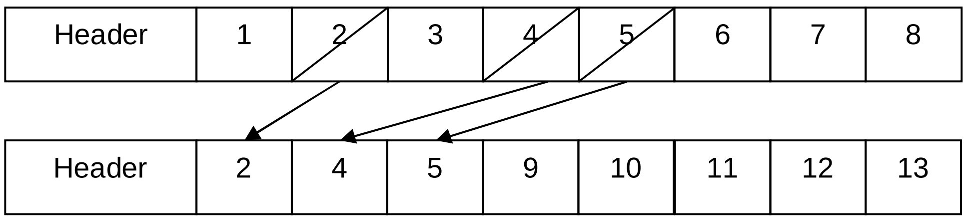


Fig. 10 Selective repeat ARQ (Auto Repeat request)

## 4. Channel Estimation

Transmission environment is a particular problem for home power line communications as shown in Figure 11. When the electrical equipment is plugged in or when the operation is started or stopped, the power supply circuit outputs various levels of noise.

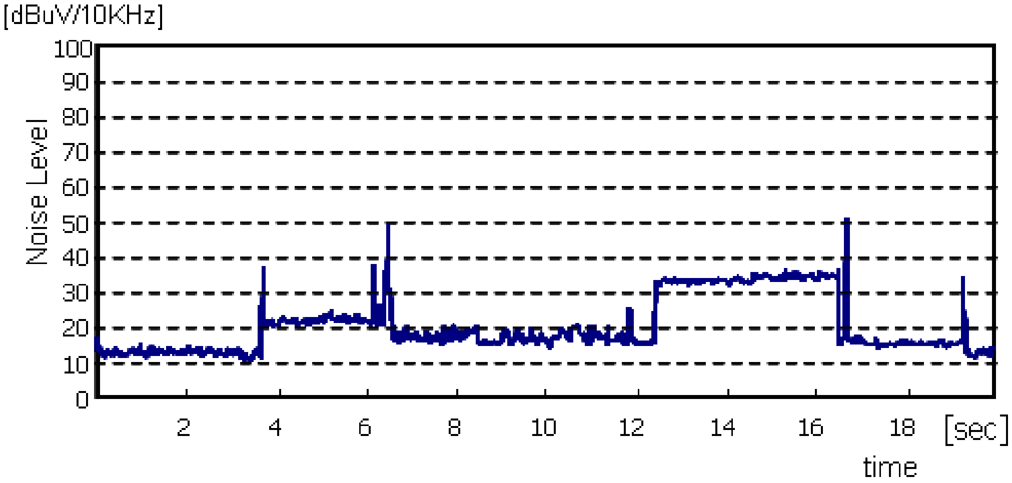


Fig. 11 transmission environment of in-home power line

The goal of the Channel Estimation (CE) procedure is to assess the channel status upon data transmission. The CE is designed to achieve the maximum throughput by effectively using power line communication media. As shown in Fig.12 HD-PLC adopts variable bit loading on each carrier for a Discrete Multi-tone (DMT) technology. It is possible to use the media effectively by estimating the channel status before and after transmission and providing information such as the best modulation parameter to a transmit terminal.

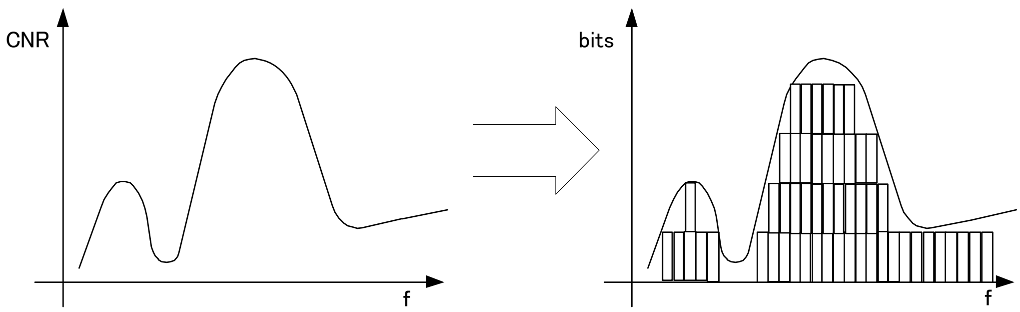


Fig. 12 Example of DMT determined by CE

 

## 5. ISP (Inter System Protocol) Overview

ISP allows power line resources to be shared among non-interoperable systems by TDM (Time Domain Multiplex). Coexistence signaling is carried out by the use of periodically repeating ISP windows that are used to convey information on coexisting system presence, resource requirements and resynchronization request. Each PLC system category is allocated a particular ISP window in a round robin fashion. ISP allows TDM to be implemented between coexisting in-home systems and an access system. The overall ISP TDM structure is shown in Figure 13. There are four such structures in every 24×AC_CYCLE.TDM resources are allocated according to the Table 2. Here HD-PLC is called IH-W.

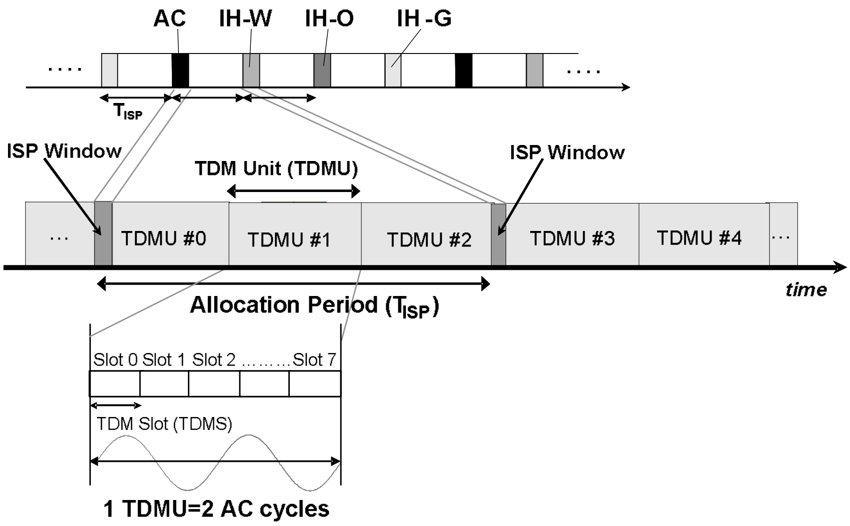


Fig. 13 General TDMA structure

Table 2 Resource allocation

| Index | ISP Field | | | | | | TDM Slot number | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ACC | IH-W | IH-O | IH-G | BW | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | - | - | - | IH-G | - | | IH-G | IH-G | IH-G | IH-G | IH-G | IH-G | IH-G | IH-G |
| 2 | - | IH-W | - | - | - | | IH-W | IH-W | IH-W | IH-W | IH-W | IH-W | IH-W | IH-W |
| 3 | - | - | IH-O | - | - | | IH-O | IH-O | IH-O | IH-O | IH-O | IH-O | IH-O | IH-O |
| 4 | - | IH-W | - | IH-G | - | | IH-W | IH-W | IH-G | IH-W | IH-W | IH-G | IH-G | IH-G |
| 5 | - | IH-W | IH-O | - | - | | IH-W | IH-W | IH-O | IH-O | IH-O | IH-W | IH-W | IH-O |
| 6 | - | - | IH-O | IH-G | - | | IH-G | IH-O | IH-O | IH-O | IH-O | IH-G | IH-G | IH-G |
| 7 | - | IH-W | IH-O | IH-G | - | | IH-W | IH-W | IH-O | IH-O | IH-O | IH-G | IH-G | IH-G |
| 8 | ACC | - | - | - | FB | | ACC | ACC | ACC | ACC | ACC | ACC | ACC | ACC |
| 9 | ACC | - | - | IH-G | PB | | IH-G | IH-G | IH-G | IH-G | ACC | ACC | IH-G | IH-G |
| 10 | ACC | - | - | IH-G | FB | | IH-G | IH-G | IH-G | ACC | ACC | ACC | ACC | IH-G |
| 11 | ACC | IH-W | - | - | PB | | IH-W | IH-W | IH-W | IH-W | ACC | ACC | IH-W | IH-W |
| 12 | ACC | IH-W | - | - | FB | | IH-W | IH-W | IH-W | ACC | ACC | ACC | ACC | IH-W |
| 13 | ACC | - | IH-O | - | PB | | IH-O | IH-O | IH-O | IH-O | ACC | ACC | IH-O | IH-O |
| 14 | ACC | - | IH-O | - | FB | | IH-O | IH-O | IH-O | ACC | ACC | ACC | ACC | IH-O |
| 15 | ACC | IH-W | - | IH-G | PB | | IH-W | IH-W | IH-G | IH-W | ACC | ACC | IH-G | IH-G |
| 16 | ACC | IH-W | - | IH-G | FB | | IH-W | IH-W | IH-G | ACC | ACC | ACC | ACC | IH-G |
| 17 | ACC | IH-W | IH-O | - | PB | | IH-W | IH-W | IH-O | IH-O | ACC | ACC | IH-W | IH-O |
| 18 | ACC | IH-W | IH-O | - | FB | | IH-W | IH-W | IH-O | ACC | ACC | ACC | ACC | IH-O |
| 19 | ACC | - | IH-O | IH-G | PB | | IH-G | IH-O | IH-O | IH-O | ACC | ACC | IH-G | IH-G |
| 20 | ACC | - | IH-O | IH-G | FB | | IH-G | IH-O | IH-O | ACC | ACC | ACC | ACC | IH-G |
| 21 | ACC | IH-W | IH-O | IH-G | PB | | IH-W | IH-W | IH-O | IH-O | ACC | ACC | IH-G | IH-G |
| 22 | ACC | IH-W | IH-O | IH-G | FB | | IH-W | IH-W | IH-O | ACC | ACC | ACC | ACC | IH-G |

 

## 6. Dynamic Notching and Dynamic power control

The dynamic notching provides reduction of interference between HD-PLC and short wave radio broadcast as shown in figure 14. The HD-PLC with dynamic notching modem will periodically sense the ingress and identify the presence of short wave radio broadcast signal. Dynamic notching works at least in the frequency allocations as defined by the ITU-R Radio Regulations or each region for radio broadcast services.
Moreover, when the HD-PLC doesn't need maximum transmission power to get good performance, the transmission power is reduced dynamically.

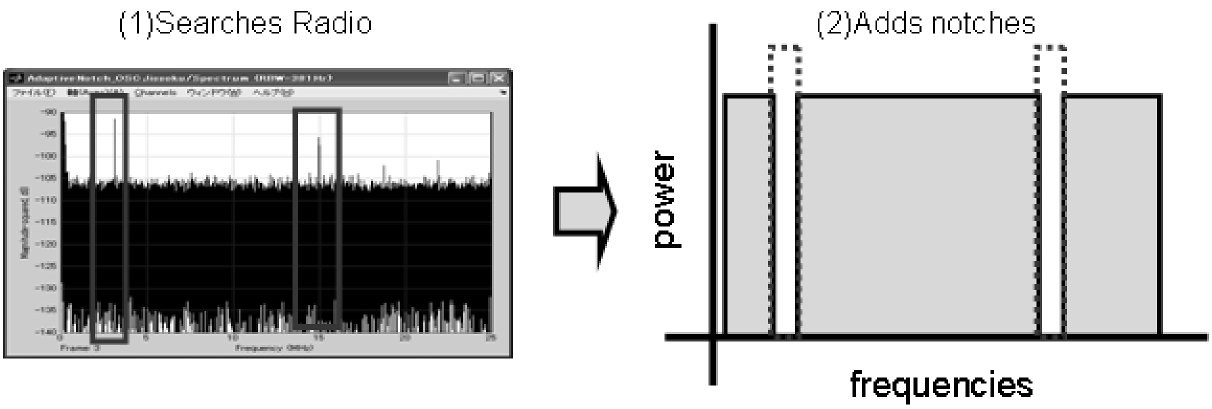


Fig. 14 Dynamic Notching

## 7. Conclusion

As described above, the HD-PLC technology is used in the PHY layer, thus achieving efficiency in high-frequency use and dynamic notches. Using QoS technology, high-speed transmission of various applications such as AV transmission and VoIP (Voice over Internet Protocol) are achieved in the MAC layer, thus allowing superiority in a stable, highly secure ubiquitous link.

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